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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/211,718	12/14/1998	ERIC R. FOSSUM	08305/015001	9540

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EXAMINER	
GENCO, BRIAN C	

ART UNIT	PAPER NUMBER
2615	27

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/211,718	FOSSUM ET AL.	
	Examiner	Art Unit	
	Brian C Genco	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 17-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Applicant's amendment filed April 15, 2004 has been fully considered by the Examiner but is not deemed persuasive.

Applicant's claim for domestic priority under 35 U.S.C. 119(e) is acknowledged. However, the provisional application upon which priority is claimed fails to provide adequate support under 35 U.S.C. 112 for claims 1-13 and 17-22 of this application. Examiner notes page 2 of Paper No. 18 wherein Examiner clearly indicated that the limitation of on-chip pixel interpolation is not supported in the provisional application number 60/069,700 filed December 16, 1997. As such, Applicant's arguments presently presented with regards to the Heller reference are moot since the Heller reference clearly qualifies as prior art under 35 U.S.C. 102(e).

Applicant's amendment has overcome the rejections previously presented based on the Schick reference.

Applicant argues that Spivey does not disclose a control portion with row selecting logic in place of a plurality of central pixels of the image sensor array.

In response, as broadly as claimed Examiner asserts that the interpretation previously presented is valid. Namely Examiner defined the top two image sensors in the first column of Fig. 17A being defined as the first image sensor and the third and forth image sensors in the first column of Fig. 17A as being the second image sensor wherein the first image sensor has row selecting logic in place of a plurality of central pixels of the image sensor array, namely row

select logic element 186, and the first and second image sensors but against one another in a coplanar manner as shown in Fig. 17B.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 2, 5-7, 9-13 and 17-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 5,886,353 to Spivey et al.) in view of (USPN 6,396,539 to Heller et al.).

In regards to claim 1 Spivey et al, herein Spivey, discloses a CMOS image sensor circuit, comprising:

a first CMOS image sensor chip including a substrate, said substrate having an image sensor portion arranged in an array of pixels of rows and columns, and a control portion with image sensor logic on said substrate, said image sensor logic being electrically connected to said image sensor portion, said image sensor logic including row logic associated with each of said rows individually, and chip logic associated with parts of said image sensor portion other than rows individually, said image sensor portion having a first area and a second area (e.g., Fig. 17A, wherein Examiner is defining the first CMOS image senor substrate as the top two sensors in the first column),

said substrate formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge (e.g., Fig. 17A, wherein the first edge is the top of the first image sensor in the first column and the second edge is the

bottom edge of the second image sensor in the first column, the third edge is edge formed alone the right side of both of the top two sensors of the first column and the fourth edge is the edge formed along the left side of both of the top two sensors of the first column),

said image sensor portion including imaging pixels extending between said first edge, said second edge, and said third edge, such that pixels of said first area of said image sensor portion are adjacent said first edge and said third edge of said substrate (e.g., image sensor portion of the top image sensor of the first column is the first area) and pixels of said second area of said image sensor portion are adjacent said second edge and said third edge of said substrate (e.g., the image sensor portion of the second image sensor in the first column is the second area. Examiner notes that Merriam Webster's Collegiate Dictionary defines the term adjacent as "not distant : nearby". Examiner further notes that the instant invention has a guard ring 103 surrounding the image sensor),

said row logic being physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor portion (e.g., the row logic element 186 of Fig. 17A is located inside said image sensor portion in place of a plurality of pixels)

a second CMOS image sensor chip configured similarly to said first CMOS image sensor chip and abutted to one of said substrate edges of said first CMOS image sensor chip (e.g., Fig. 17A)

It is also known in the art to use on-chip pixel interpolation as taught by Heller et al, herein Heller. Heller discloses having an on-chip memory and controller unit for storing defective pixel locations so that the controller can interpolate values for the defective pixels from the surrounding pixels (e.g., column 8, lines 39-65; column 4, lines 5-9). Note that Heller discloses that it is preferable to include as much circuitry on-chip in order to reduce cost (column

1, line 56 – column 2, line 36). While Spivey discloses using pixel interpolation this process is done off-chip, therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have preformed pixel interpolation on-chip in order to reduce cost. Furthermore it would have been obvious to one of ordinary skill in the art at the time of the invention to have place the pixel interpolator between said image area and said fourth edge so as to still enable butting for the creation of a large format array as taught by Spivey.

In regards to claim 2 Examiner notes column 11, line 55 – column 12, line 5 wherein it is disclosed that each pixel is 66 microns wide and the row-select shift register 186 is about 100 microns wide, thus it is formed in place of two columns of the array.

In regards to claim 5 see Examiners notes on the rejection of claim 1 and note column 15, lines 30-37 of Spivey's disclosure.

In regards to claim 6 see Examiners notes on the rejection of claim 1.

In regards to claim 7 note edge element 189.

In regards to claims 9-13, 17-21 see Examiners notes on the rejection of claim 1.

In regards to claims 11 and 18 note that the claimed limitation of integrating the control portions of said at least two CMOS image sensors in inherent with providing a large format image sensor as disclosed by Spivey.

In regards to claim 19 see Examiners notes on the rejection of claim 2.

In regards to claim 20 Spivey discloses providing lead shielding for the read-out circuit and as such it is non-photosensitive (column 19, lines 3-17).

In regards to claim 21 see Fig. 17A wherein the row logic divides the image sensor as defined above into a first and second area.

In regards to claim 22 see Examiners notes on the rejection of claim 1. Note Fig. 17B wherein abutted image sensors of the same column are co-planar.

Claims 3, 4, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 5,886,353 to Spivey et al.) in view of (USPN 6,396,539 to Heller et al.) in further view of (US PG PUB 20020000549 to Spartiotis et al.).

In regards to claim 3 Examiner notes column 11, line 55 – column 12, line 5, wherein two pixel pitches is 132 microns, wherein the largest distance between said image sensor portion is between the image sensor portion and the second edge as defined above. Examiner notes that the row-select shift register 186 has a width of about 100 microns. Examiner further notes that the edge 189 is less than 250 microns. In order for the image sensor portion and the second edge to be within two pixel pitches then the edge 189 must be 32 microns or less. Examiner notes that 32 microns or less is less than 250 microns. Examiner notes that Spivey discloses that the edge of the array is cut to facilitate butting using a diamond saw. Examiner notes that Spartiotis et al, herein Spartiotis, discloses that it is preferable to minimize the spacing between the image sensor and the edge (e.g., paragraph 0008). This is shown by having a edge spacing of 30 microns (e.g., paragraph 0009). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have cut Spivey's sensor so that the border region 189, or edge spacing, was 30 microns in order to minimize the spacing between image sensors. This is further evidenced by Spartiotis disclosure that modern cutting techniques for diamond saws have a precision of 10-20 microns.

In regards to claim 4 see Fig. 17A and the rejection to claim 1.

In regards to claim 8 Spivey discloses a method of operating a large format image sensor, comprising:

first obtaining an image sensor chip which has first and second edges and an image sensor array of imaging pixels that comes within two pixel pitches of said first and second edges and includes a control portion with row selecting logic in place of a plurality of central pixels of the image sensor array (e.g., Fig. 17A wherein the first edge is the top of the first image sensor in the first column and the second edge is the bottom of the second image sensor in the first column. Examiner notes column 11, line 55 – column 12, line 5, wherein two pixel pitches is 132 microns, wherein the largest distance between said image sensor portion and an edge is between the image sensor portion and the second edge as defined above. Examiner notes that the row-select shift register 186 has a width of about 100 microns. Examiner further notes that the edge 189 is less than 250 microns. In order for the image sensor portion and the second edge to be within two pixel pitches then the edge 189 must be 32 microns or less. Examiner notes that 32 microns or less is less than 250 microns. Examiner notes that Spivey discloses that the edge of the array is cut to facilitate butting using a diamond saw. Examiner notes that Spartiotis et al, herein Spartiotis, discloses that it is preferable to minimize the spacing between the image sensor and the edge (e.g., paragraph 0008). This is shown by having a edge spacing of 30 microns (e.g., paragraph 0009). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have cut Spivey's sensor so that the border region 189, or edge spacing, was 30 microns in order to minimize the spacing between image sensors. This is further evidenced by Spartiotis disclosure that modern cutting techniques for diamond saws have a precision of 10-20 microns.), and includes a control portion with row selecting logic in place of a

plurality of central pixels of the image sensor, and an image portion divided into two areas (e.g., row selecting element 186 of Fig. 17A);

abutting said image sensor chip against a similar image sensor chip of corresponding construction (e.g., Fig. 17A); and

interpolating missing pixels, the missing pixels being caused by both said row select logic and by spaces between said image sensor chips (e.g., column 15, lines 30-37).

Examiner notes that neither Spivey nor Spartiotis disclose performing on-chip pixel interpolation. It is known in the art to use on-chip pixel interpolation as taught by Heller. Heller discloses having an on-chip memory and controller unit for storing defective pixel locations so that the controller can interpolate values for the defective pixels from the surrounding pixels (e.g., column 8, lines 39-65; column 4, lines 5-9). Note that Heller discloses that it is preferable to include as much circuitry on-chip in order to reduce cost (column 1, line 56 – column 2, line 36). While Spivey discloses using pixel interpolation this process is done off-chip, therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have preformed pixel interpolation on-chip in order to reduce cost.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian C. Genco who can be reached by phone at 703-305-7881 or by fax at 703-746-8325. The examiner can normally be reached on Monday thru Friday 8:30am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on 703-308-9644. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the customer service office whose telephone number is 703-308-4357.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian C Genco
Examiner
Art Unit 2615

June 28, 2004

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